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10/803,011	03/17/2004	Babak A. Taheri	5298-18200	4386

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,011	TAHERI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13,15-21 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6,8 and 9* is/are allowed.

6)☒ Claim(s) *10-13,15-17,19-21 and 23-25* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 09 March 2006. The changes and remarks disclosed therein have been considered.

Claims 7, 14 and 22 have been cancelled by Amendment. Therefore, claims 1-6, 8-13, 15-21 and 23-25 are pending in the application.

Specification

2. Claim 10 is objected to because of the following informalities:

In claim 10, line 9, "the pair of cross-coupled transistors" appear to be referring to "a pair of cross-coupled inverters" in lines 2-3 of the claim, and will be understood as such.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 20, 21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cuevas (U.S. Pat. No. 5,097,449) in view of Roohparvar et al. (U.S. Pat. No. 6,141,247).

Regarding claim 20, Cuevas, for example in Fig. 1, discloses a method for programming a programmable storage element (within 40), comprising: latching a voltage value from a data

bus (D and /D) onto an output of a pair of cross-coupled inverters (42); forwarding the latched voltage value onto a gate of a selecting transistor (53 or 51) to activate the selecting transistor; and driving current (to program the floating nodes 21) from the programmable storage element through the activated selecting transistor to a ground supply conductor (see Fig. 1 which shows 53 and 51 providing paths to ground Gnd depending on the gate voltages).

Cuevas does not disclose that said forwarding comprises placing the voltage value onto the gate of the selecting transistor during times when a source-to-drain path of a programming transistor is activated via a programming voltage placed on a gate of the programming transistor.

Roohparvar, in Figs. 1 and 2, discloses a source-to-drain path of a programming transistor (24 or 26 in Fig. 1) being activated via a programming voltage (CN) placed on a gate of the programming transistor (see the program cycle in Fig. 2).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the method of Cuevas by including a programming transistor between the latch and the programmable storage element (as in Roohparvar), such that the voltage value would be placed onto the gate of the selecting transistor during times when a source-to-drain path of a programming transistor is activated via a programming voltage placed on a gate of the programming transistor, for the purpose of providing a greater flexibility in controlling the transfer of data between the latch and the programmable storage element for programming and other operations (see for example Roohparvar, Fig. 2 and column 1, line 58 through column 2, line 5).

Regarding claims 21 and 23-25, the above combination further discloses that said forwarding comprises placing the voltage value that is greater than a threshold voltage above a ground supply onto the gate of the selecting transistor whose source terminal is coupled to the ground supply via the ground supply conductor (see 53 and 51 connections in Fig. 1 of Cuevas);

wherein said driving comprises sending current across a gate oxide of a programmable transistor (including the floating nodes 21 in Fig. 1 of Cuevas) that forms the programmable storage element and through the source-to-drain path of the selecting transistor (53 or 51) having a gate oxide dissimilar than the gate oxide of the programmable transistor (since the gate oxide of the programmable transistor involves tunneling, while that of the selecting transistor does not);

wherein said driving comprises sending current from the programmable storage element through a path (the ground path through the transistors 53 or 51 in Fig. 1 of Cuevas) outside the pair of cross-coupled inverters (i.e., no current from the storage element within 40 flows through the latch 42);

wherein said latching comprises maintaining the voltage value onto the output (Q and /Q in Fig. 1 of Cuevas) of the pair of cross-coupled inverters (42) after the voltage value from the data bus (D and /D) terminates (inherent property of the cross-coupled inverters).

5. Claims 10, 12, 13, 15-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cuevas (U.S. Pat. No. 5,097,449) in view of Naura et al. (U.S. Pat. No. 5,999,447), Casper et al. (U.S. Pat. No. 5,812,477), Kothandaraman (U.S. Pat. No. 6,617,914) and Roohparvar et al. (U.S. Pat. No. 6,141,247).

Regarding claim 10, Cuevas, for example in Fig. 1, discloses a programmable latching circuit, comprising: a latch (42) having two pairs of latching transistors connected to form a pair of cross-coupled inverters (the configuration of 42); a pair of programmable storage elements (within 40) coupled to respective outputs (Q and /Q) of the inverters, wherein the storage elements include a pair of storing transistors (45 and 46) having a gate oxide thickness (associated with tunneling; see for example column 3, lines 8-19) dissimilar from a gate oxide thickness of any of the set of latching transistors; and a selection circuit that includes gates of a pair of selecting transistors (53 and 51) coupled to inputs of the pair of cross-coupled inverters (within 42).

Cuevas does not disclose that the storage element comprises a one-time programmable (OTP) storage element that includes a pair of storing transistors having a gate oxide thickness dissimilar from a gate oxide thickness of any of the set of latching transistors; and a pair of programming transistors with source-to-drain paths coupled between said inputs of the pair of cross-coupled inverters and said gates of the pair of selecting transistors.

Naura discloses one-time programmable (OTP) storage elements in non-volatile memory devices (see for example column 1, lines 11-40).

Casper, for example in Fig. 3, discloses a pair of complementary antifuses (100 and 102; see also Figs. 4-6) as OTP storage elements (antifuses are inherently OTP).

Kothandaraman, for example in Figs. 1 and 3, discloses a MOSFET (a transistor) configured as an antifuse (or as a storing transistor) (see also column 1, lines 20-42 and column 3, lines 3-19).

Roohparvar, in Figs. 1 and 2, discloses a pair of programming transistors (24 and 26 in Fig. 1) with source-to-drain paths coupled between inputs of a pair of cross-coupled inverters (within 12) and a pair of nonvolatile storage elements (within 10).

Since Casper's antifuses and Cuevas' EEPROMs have similar programming circuits and operations (for example, in Casper, Fig. 3, the programming ground paths for the storage elements are provided through a pair of transistors 130(a)-(b) controlled by data voltages on their gates, similar to that disclosed in Cuevas, Fig. 1; see also Casper, column 4, lines 8-32), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute Cuevas' EEPROM storage elements with a pair of complementary OTP antifuses (similar to those of Casper), for the purpose of storing permanent information that is written once and that cannot be easily overwritten or erased, such as manufacturing batch number, the data of manufacture, etc. (see for example Naura column 1, lines 11-40).

Further, since use of MOSFET structures for antifuses (or storing transistors) was common and well known in the art (as exemplified in Kothandaraman), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use MOSFET-based antifuses (or storing transistors), as an art-recognized equivalent antifuse structure, with a gate oxide thickness dissimilar from a gate oxide thickness of any of the set of latching transistors, since discovering the optimum or workable ranges, or an optimum value of a result effective variable (e.g., the gate oxide thickness of the storing transistor antifuse, depending on the desired programming voltage) involves only routine skill in the art.

In addition, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a pair of programming transistors between said latch

and said pair of programmable storage elements (as in Roohparvar), such that the source-to-drain paths of the programming transistors would be coupled between the inputs of the pair of cross-coupled inverters and the gates of the pair of selecting transistors, for the purpose of providing a greater flexibility in controlling the transfer of data between the latch and the storage element for programming and other operations (see for example Roohparvar, Fig. 2, and column 1, lines 58 through column 2, line 5).

Regarding claims 12, 13, 15-17 and 19, the above combination further discloses that the circuit is formed using a fabrication process that avoids additional steps or features needed to accommodate programming voltages that exceed twice the voltages on the latch (i.e., in Cuevas, because the latch 42 and the storage element within 40 are essentially isolated via gate connections at the transistors 53 and 51, any additional features for the latch to accommodate any large voltage/current from the storage element are not needed);

a data bus (D and /D in Fig. 1 of Cuevas) coupled to inputs of the pair of cross-coupled inverters (via 41 and 41');

the programming transistors including a gate terminal adapted to receive a programming voltage (CN in Figs. 1 and 2 of Roohparvar) and, upon receiving the programming voltage, one of the programming transistors causes a binary value on the data bus (via Q and /Q in Fig. 1 of Cuevas) to be placed on a gate of one of the pair of selecting transistors (53 and 51 in Fig. 1 of Cuevas, or equivalently 130(a)-(b) in Fig. 3 of Casper, in the combination) causing programming current to flow from one of the pair of storage elements (100 and 102 in Fig. 3 of Casper),

through one of the pair of selecting transistors, and directly to a ground supply conductor configured within the latching circuit outside the latch (see Fig. 1 of Cuevas or Fig. 3 of Casper);

the latch comprising a holding transistor (to control Vsup in Fig. 1 of Roohparvar; see also Fig. 2) coupled between each of the two pair of latching transistors (in 12) to maintain a latched voltage value on the output of the pair of cross-coupled inverters during times when the holding transistor is activated (i.e., Vsup is at a high voltage to render the latch functional; see Figs. 1 and 2 of Roohparvar); and

the one-time programmable storage element comprising a dielectric that (i) upon receiving a programming voltage differential across the dielectric a relatively low resistive path will occur to a power supply, and (ii) upon receiving a non-programming voltage differential across the dielectric a relatively high resistive path will occur to the power supply (inherent in antifuses; see also Casper, column 1, lines 21-29).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cuevas in view of Naura et al., Casper et al., Kothandaraman and Roohparvar et al. as applied to claim 10 above, and further in view of Ahn et al. (U.S. Pat. No. 6,297,103).

Regarding claim 11, the above Cuevas/Naura/Casper/Kothandaraman/Roohparvar combination discloses a one-time programmable latching circuit as recited in claim 10, with the exception of the circuit being formed using a fabrication process capable of forming sub one-quarter micron features.

Ahn discloses a fabrication process capable of forming sub one-quarter micron features (see for example column 2, lines 33-41).

Since sub one-quarter micron fabrication process was well known in the art (as disclosed in Ahn), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to form the circuit of the above combination using a fabrication process capable of forming sub one-quarter micron features, for the purpose of reducing the size of the circuit elements and thus increasing the circuit density on a substrate.

Allowable Subject Matter

7. Claims 1-6, 8 and 9 are allowed.

8. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The record of the prosecution as a whole makes clear the reasons for the indication of allowable subject matter (particularly, for claim 1, see the previous Office Action and the reason for claim 7, the subject matter of which is incorporated into claim 1).

Response to Arguments

9. Applicant's arguments filed 09 March 2006 have been fully considered but they are not persuasive.

With respect to claim 20, Applicant argues, in the middle paragraph on page 7, that "the connect signal is not a programming voltage."

In response, it is noted that Roohparvar in Fig. 2 discloses a CN voltage pulse that is unique to the program cycle; thus, such voltage is interpreted as "a programming voltage."

Applicant further argues, in the same paragraph, that "nowhere in Roohparvar is there any mention that the source-to-drain path of transistor 24/26 connects the output from latch 12 to a gate of a pair of selecting transistors" (emphasis added by Applicant).

In response, it is noted that the combination of Cuevas and Roohparvar would have a source-to-drain path of a transistor (similar to 24 or 26 in fig. 1 of Roohparvar) connect the output from a latch (42 in Fig. 1 of Cuevas) to a gate of a pair of selecting transistors (53 and 51 in Fig. 1 of Cuevas). See the rejections above.

Applicant further argues, in the last paragraph on page 7, that the combining of Cuevas and Roohparvar is not obvious "unless the prior art suggested the desirability of that combination" and that "a skilled artisan looking at Cuevas and finding no source-to-drain path to a gate of a selecting transistor would not assume that the missing source-to-drain path can be supplanted with a source-to-drain path, not to a gate but to a drain in Roohparvar, to somehow meet the present claims."

In response, it is noted that the transistors 24 and 26 in Fig. 1 of Roohparvar control the connectivity or transfer of data between a volatile memory device (LATCH in Fig. 1 of Roohparvar) and a nonvolatile memory device (FLASH) during program and recall cycles (see Fig. 2 of Roohparvar); therefore, one of ordinary skill in the art would be motivated to include such transistors between Cuevas' volatile and nonvolatile devices, to provide a greater flexibility in controlling the connectivity or the transfer of data between Cuevas' volatile and nonvolatile devices. Such motivation/desirability is implied, for example, in Roohparvar, column 1, line 58

through column 2, line 5, and considered to be found in the knowledge generally available to one of ordinary skill in the art.

Similar argument, presented with respect to claim 10 on page 9, is moot in light of the above response.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER